What is claimed is:

1. A plasma display panel comprising:

a plurality of sustain electrode pairs successively formed on an upper electrode;

a plurality of common electrodes formed one by one between a pair of the sustain electrodes; and

a dielectric layer formed on the substrate to deposit the sustain electrodes and the common electrodes.

2. The plasma display panel of claim 1, wherein the common electrodes are commonly connected to a common node.

3. The plasma display panel of claim 1, wherein the common electrodes are formed of a three-layered structure of Cr, Cu, and Cr sequentially deposited on the substrate.

4. The plasma display panel of claim 1, wherein the common electrodes are formed of Ag.

5. The plasma display panel of claim 1, wherein the dielectric layer has a thickness of 10μm to 30μm.

6. The plasma display panel of claim 1, further comprising black matrixes formed between the substrate and the common

electrodes.

7. A method for driving a plasma display panel which includes a plurality of sustain electrode pairs successively formed on a substrate, a plurality of common electrodes between a pair of the sustain electrodes, and a plurality of address electrodes formed to cross the sustain electrodes, the method comprising the steps of:

applying a common pulse, which is periodically turned on/off, to the common electrodes;

applying a scan pulse to one of a pair of the sustain electrodes; and

applying an address pulse to the address electrodes when the scan pulse is applied to the one sustain electrode.

8. The method of claim 7, wherein the potential difference between on/off-periods of the common pulse is lower than a discharge start voltage of the plasma display panel.

9. The method of claim 8, wherein the potential difference is 270V or below.

10. The method of claim 7, wherein a width of the common pulse in the on-period is 1μs or below.

11. The method of claim 7, wherein the maximum potential difference between the scan pulse and the address pulse is more than the discharge start voltage of the plasma display panel.

12. The method of claim 7, wherein the maximum potential difference between the scan pulse and the address pulse is more than 280V.

13. The method of claim 7, wherein the time difference between the time when the common pulse is turned off and the time when the scan pulse is turned on is 500ns or below.

14. The method of claim 7, wherein the time difference between the time when the common pulse is turned off and the time when the address pulse is turned on is 500ns or below.

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